中国中车 CRRC

TMTC,TMTD 700

Ver：2021C. 2

Thyristor,Diode Modules

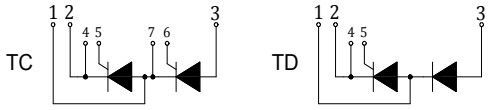
Key Parameters

V_{RRM}	**1400**	**V**
$I_{T(AV)}$	**700**	**A**
I_{TSM}	**21**	**kA**
V_{TO}	**0.85**	**V**
r_T	**0.22**	**mΩ**

Applications

- Various rectifiers
- DC supply for PWM inverter
- Industry converter

- 3000 V_{RMS} isolating voltage with baseplate
- High power capability
- Industrial standard package



Voltage Ratings

Module Type	V_{DRM}/V_{RRM}(V)	Test Conditions
TMTC 700	1400	T_{vj} = 25，130 °C $I_{DRM} = I_{RRM} \leq$ 150 mA $V_{DM} = V_{DRM}$ $V_{RM} = V_{RRM}$ t_p = 10 ms $V_{DSM} = V_{DRM}$ $V_{RSM} = V_{RRM}$ + 100

Thermal & Mechanical Data

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
$R_{th(J-C)}$	Thermal Resistance junction to case	sine.180°, per chip / per module DC , per chip / per module	-	-	0.064 / 0.032 0.061/ 0.03	K / W
$R_{th(C-H)}$	Thermal resistanc case to heatsink	per chip / per module	-	-	0.02 / 0.01	K / W
T_{vj}	Maximum junction temperature		-	-	135	°C
$T_{c\,op}$	operating temperature		-40	-	130	°C
T_{stg}	Storage temperature		-40	-	130	°C
F	Busbar to module M10	Mounting torque ± 10 %	-	12	-	N·m
	Module to heatsink M6		-	6	-	N·m
W	Weight		-	1.5	-	kg
S	Creepage distance		-	19	-	mm
a	virbration resistance		-	50	-	m/s²

Current Ratings

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
$I_{T(AV)}$	Mean on-state current	Half Sine Wave, T_C=85°C Half Sine Wave, T_C=80°C	-	-	650 703	A
$I_{T(RMS)}$	RMS on-state current	T_C =85℃	-	-	1021	A
I_{TSM}	Surge on-state current	t_p=10ms, Half Sine Wave, T_{vj}=25°C, V_R = 0	-	-	21.0	kA
I^2t	Limiting load integral	Sine Wave, t_p=10ms	-	-	221	10^4A^2s

Characteristics

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
V_{TM}	Peak on-state voltage	T_{vj} = 25°C， I_{TM} = 1950 A	-	-	1.4	V
		T_{vj} = 130 °C， I_{TM} = 1950 A	-	-	1.34	
I_{DRM}	Forward leakage current	T_{vj} = 25 °C， 130 °C， V_{DRM}/V_{RRM}	-	-	150	mA
I_{RRM}	Reverse leakage current					
V_{isol}	Isolation voltage	a.c.; 50 Hz; r.m.s. ; t =1min	-	3000	-	V
V_{TO}	Threshold voltage	T_{vj} = 130 °C	-	-	0.85	V
r_T	Slope resistance	T_{vj} = 130 °C	-	-	0.22	mΩ
I_H	Holding current	T_{vj} = 25 °C	-		200	mA
I_L	Latching current	T_{vj} = 25 °C	-	-	1000	mA

Dynamic Parameters

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
dv/dt	Critical rate of rise of off-state voltage	T_{vj} = 130 ℃， *Exp*. to 0.67 V_{DRM}	1000	-	-	V/μs
di/dt	Critical rate of rise of on-state current	T_{vj} = 130 °C， V_{DM} = 0.67 V_{DRM}， f = 50 Hz I_{TM} = 1000 A， I_{FG} = 2 A， t_r = 0.5 μs	-	-	250	A/μs
t_q	Turn-off time	T_{vj} = 130 °C， V_{DM} = 0.67 V_{DRM}， I_T = I_{TMAX} *dv/dt* = 20 V /μs， V_R = 200 V， *-di/dt* = 10 A/μs	-	150	-	μs
Q_{rr}	Reverse Recovery Charge	T_{vj} = 130 °C， *-di/dt* = 10 A/μs， I_T = I_{TM}， V_R = 200 V	-	1000	-	μC

Gate Parameters

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
I_{GT}	Gate trigger current	T_{vj} = 25 ℃	200	-	-	mA
V_{GT}	Gate trigger voltage	T_{vj} = 25 ℃	-	-	3	V
V_{GD}	Gate non-trigger voltage	T_{vj} = 130 ℃， V_D = 0.4V_{DRM}	0.3	-	-	V
V_{FGM}	Peak forward gate voltage		-	-	12	V
V_{RGM}	Peak reverse gate voltage		-	-	5	V
P_{GM}	Gate peak power losses		-	-	20	W
$P_{G(AV)}$	Gate average power losses		-	-	4	W

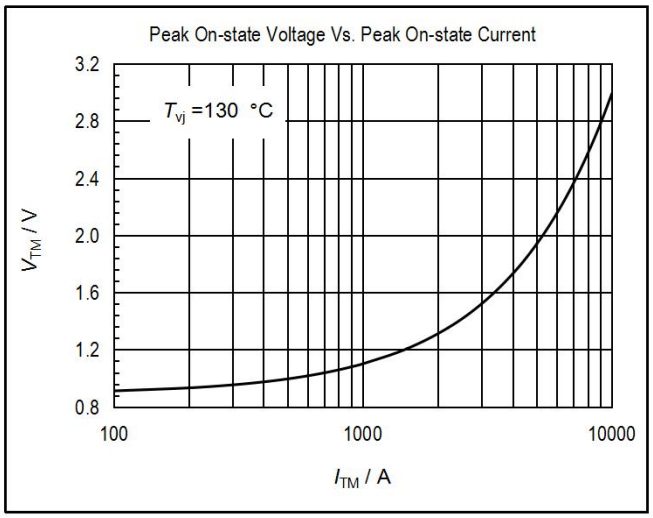


Fig1. Peak on-state Voltage Vs. Peak On-state Current

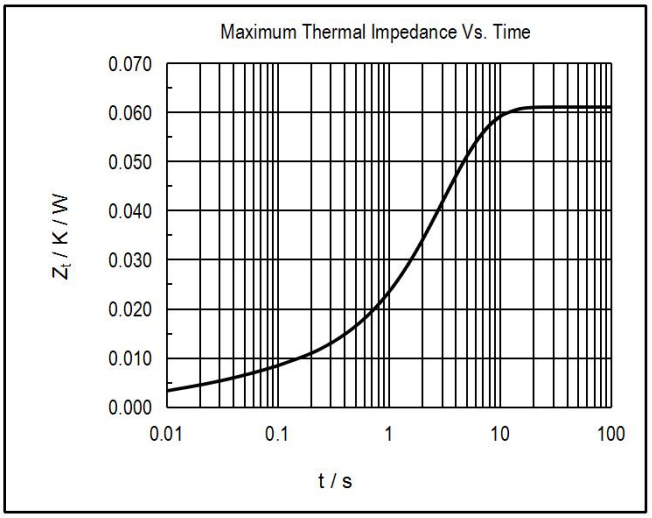


Fig2. Transinent thermal Impedance Vs. Time

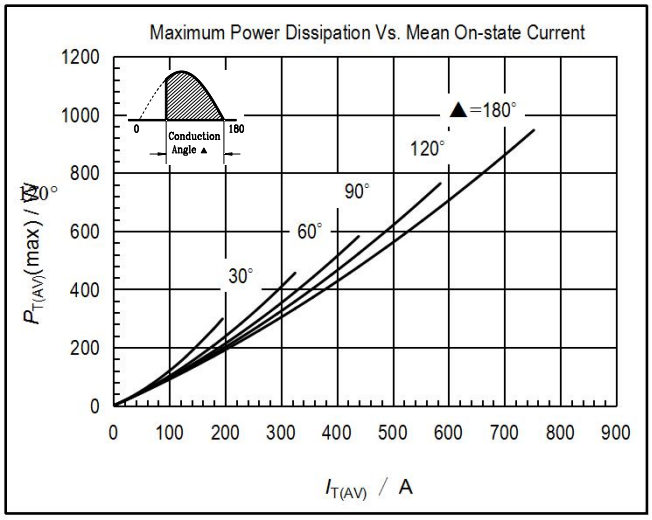


Fig3. Maximum Power Dissipation Vs. Mean On-state Current

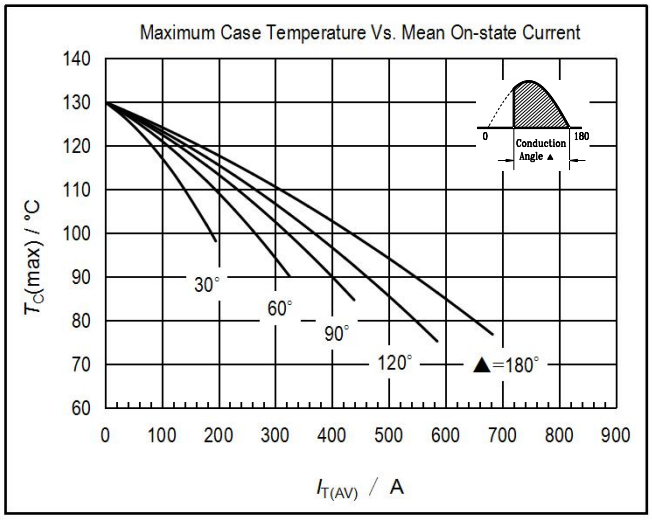


Fig4. Maximum Case Temperature Vs. Mean On-state Current

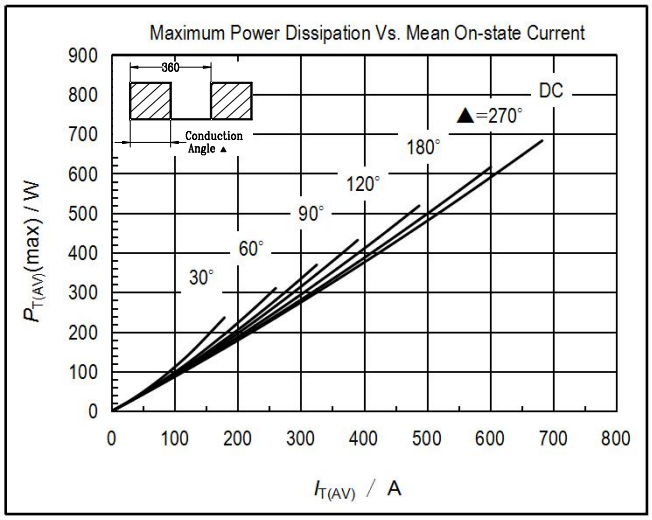


Fig5. Maximum Power Dissipation Vs. Mean On-state Current

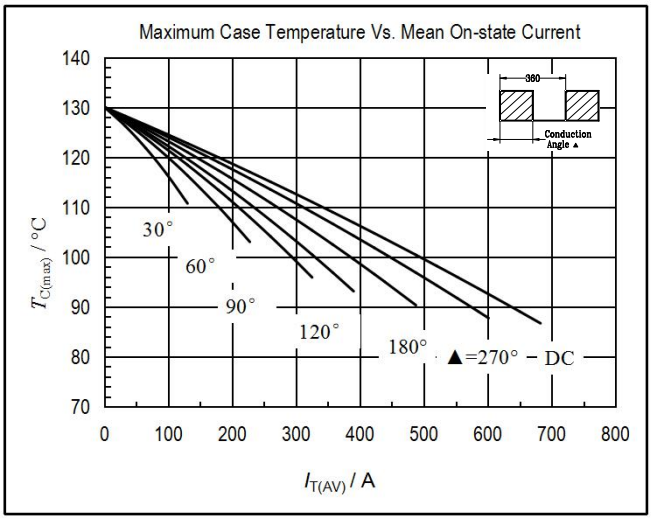


Fig6. Maximum Case Temperature Vs. Mean On-state Current

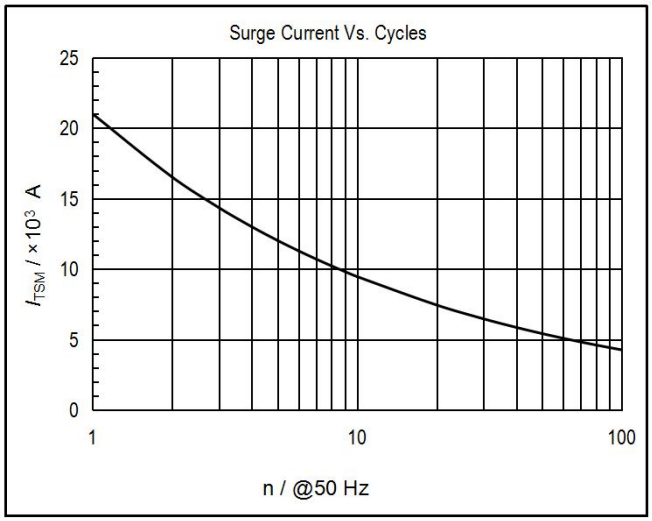


Fig7. Surge Current Vs. Cycles

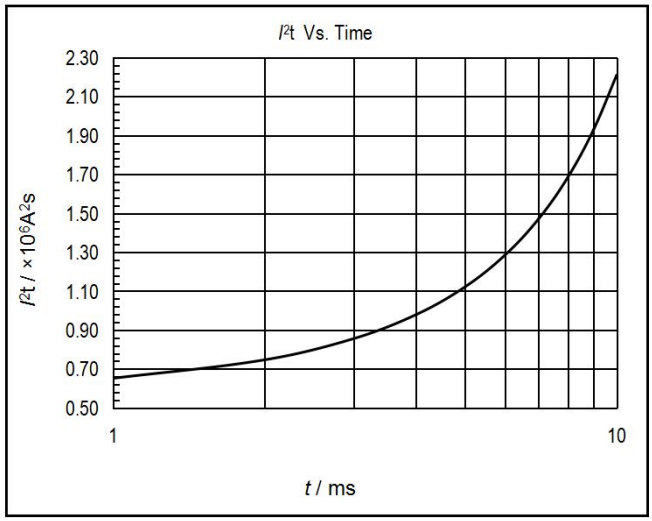


Fig8. I^2t Vs. Time

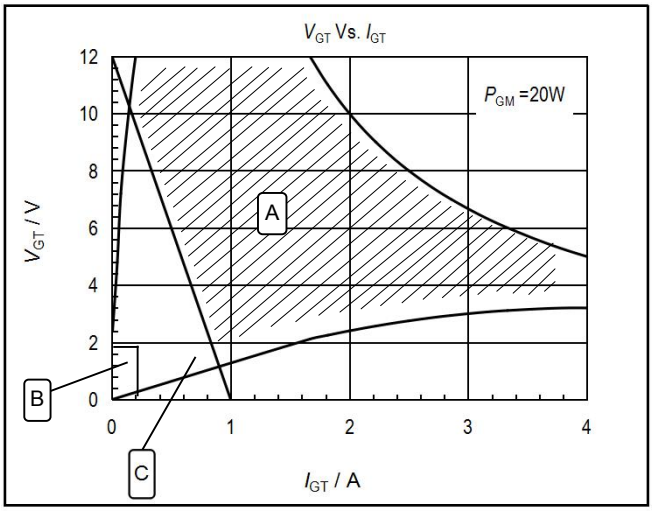


Fig9. V_{GT} Vs. I_{GT}

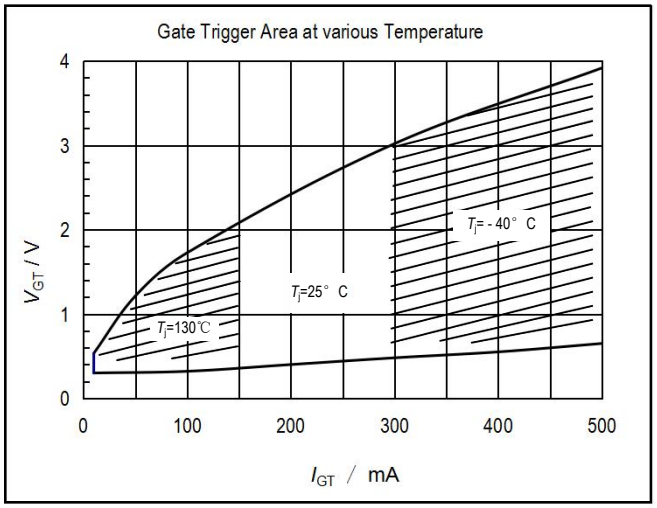


Fig10. Gate Trigger Area at various Temperature

A is Recommended Triggering Area.
B is Unreliable Triggering Area.
C is Recommended Gate Load Line.

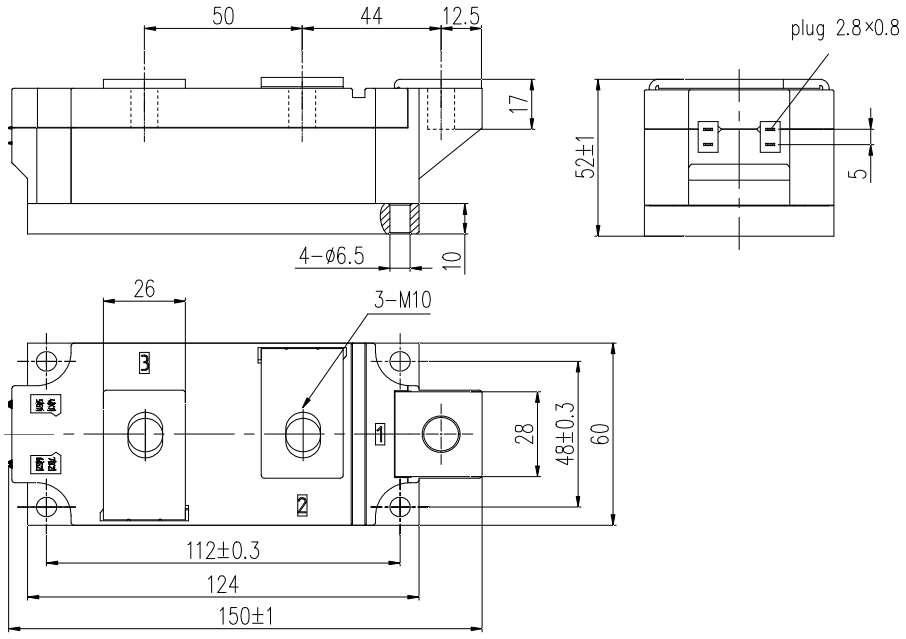


Fig9.Outline

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